IN THE CLAIMS

1. (Previously Presented) A thin film transistor comprising:

a gate electrode;

a gate insulating layer formed on the gate electrode;

a semiconductor layer formed on the gate insulating layer and disposed opposite the gate electrode;

a source electrode and a drain electrode that are formed at least in part on the semiconductor layer and face each other;

a passivation layer formed on the source electrode, the drain electrode, and a portion of the semiconductor layer that is not covered with the source electrode and the drain electrode; and

a shielding electrode formed on the passivation layer and disposed on a region between the source electrode and the drain electrode,

wherein the shielding electrode provides voltage shielding for the region on which it is disposed, and

wherein the shielding electrode comprises a transparent electrode.

2. (Original) The thin film transistor of claim 1, wherein the shielding electrode is electrically isolated.

3. (Original) The thin film transistor of claim 1, wherein the shielding electrode is supplied with a predetermined voltage.

4. (Original) The thin film transistor of claim 3, wherein the predetermined voltage supplied to the shielding electrode is equal to or lower than a ground voltage.

5. (Original) The thin film transistor of claim 3, wherein the predetermined voltage supplied to the shielding electrode is a negative voltage.

HAYNES AND BOONE, LLP>
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

6. (Original) The thin film transistor of claim 1, wherein the shielding electrode comprises IZO or ITO.

7. (Original) The thin film transistor of claim 1, wherein the shielding electrode has a shape of horseshoes.

8. (Original) The thin film transistor of claim 1, wherein the passivation layer comprises organic insulator.

9. (Previously Amended) A thin film transistor array panel comprising:

a gate line and a data line;

a first thin film transistor including a control electrode, an input electrode, an output electrode, and a channel portion disposed between the input electrode and the output electrode and generating a gate signal to be applied to the gate line;

a second thin film transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, a drain electrode, and a channel portion disposed between the source electrode and the drain electrode and transmitting a data signal from the data line in response to the gate signal from the gate line;

a pixel electrode connected to the drain electrode to receive the data signal; ~~and~~

a first shielding electrode disposed on the channel portion of the first thin film transistor, wherein the first shielding electrode is formed of the same layer as the pixel electrode.

10. (Original) The thin film transistor array panel of claim 9, wherein the first shielding electrode is electrically isolated.

11. (Original) The thin film transistor array panel of claim 9, wherein the first shielding electrode is supplied with a predetermined voltage.

HAYNES AND BOONE, LLP>
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

12. (Original) The thin film transistor array panel of claim 11, wherein the predetermined voltage supplied to the first shielding electrode is equal to or lower than a ground voltage.

13. (Original) The thin film transistor array panel of claim 11, wherein the predetermined voltage supplied to the first shielding electrode is a negative voltage.

14. (Original) The thin film transistor array panel of claim 11, wherein the predetermined voltage supplied to the first shielding electrode has a magnitude for turning off the second thin film transistor.

15. (Cancelled).

16. (Original) The thin film transistor array panel of claim 9, further comprising a second shielding electrode disposed on the channel portions of the second thin film transistor and including the same layer as the pixel electrode.

17. (Original) The thin film transistor array panel of claim 16, further comprising an insulating layer disposed between the first and the second thin film transistors and the first and the second shielding electrodes.

18. (Original) The thin film transistor array panel of claim 17, wherein the insulating layer comprises organic material.

19. (Currently Amended) A display device comprising:

a gate line and a data line;

a first thin film transistor including a gate electrode, a source electrode, a drain electrode, and a channel portion disposed between the source electrode and the drain electrode and generating a gate signal to be applied to the gate line;

a second thin film transistor transmitting a data signal from the data line in

HAYNES AND BOONE, LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

response to the gate signal from the gate line;

a pixel electrode connected to the second thin film transistor to receive the data signal;

a shielding electrode disposed on the channel portion between the source electrode and the drain electrode of the first thin film transistor, wherein the shielding electrode is formed of the same layer as the pixel electrode; and

a common electrode facing the pixel electrode.

20. (Original) The display device of claim 19, wherein the shielding electrode faces the common electrode.

21. (Original) The display device of claim 20, wherein the shielding electrode is supplied with a predetermined voltage lower than a voltage applied to the common electrode.

22. (Original) The display device of claim 21, wherein the predetermined voltage supplied to the shielding electrode has a magnitude for turning off the second thin film transistor.

23. (Cancelled).

24. (Previously Presented) The display device of claim 19 further comprising a dielectric layer disposed between the shielding electrode and the common electrode.

25. (Original) The display device of claim 24, wherein the dielectric layer comprises a liquid crystal layer.

HAYNES AND BOONE, LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

26. (Previously Presented) The thin film transistor of claim 1, wherein the shielding electrode is formed on a channel portion of the thin film transistor.

27. (New) A thin film transistor array panel comprising:

a gate line and a data line;

a first thin film transistor including a control electrode, an input electrode, an output electrode, and a channel portion disposed between the input electrode and the output electrode and generating a gate signal to be applied to the gate line;

a second thin film transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, a drain electrode, and a channel portion disposed between the source electrode and the drain electrode and transmitting a data signal from the data line in response to the gate signal from the gate line;

a pixel electrode connected to the drain electrode to receive the data signal; and

a second shielding electrode disposed on the channel portion between the source electrode and the drain electrode of the second thin film transistor, wherein the second thin film transistor is formed of the same layer as the pixel electrode.

28. (New) The thin film transistor array panel of claim 27, further comprising a first shielding electrode disposed on the channel portion between the source electrode and the drain electrode of the first thin film transistor, wherein the first thin film transistor is formed of the same layer as the pixel electrode.

29. (New) The thin film transistor array panel of claim 27, wherein the second shielding electrode is electrically isolated.

30. (New) The thin film transistor array panel of claim 27, wherein the second shielding electrode comprises a transparent electrode.

31. (New) The thin film transistor array panel of claim 27, wherein the second shielding electrode is supplied with a predetermined voltage.

HAYNES AND BOONE, LLP>
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262